What is claimed is:

1. A substrate panel for use in semiconductor packaging, comprising:

a lead-frame panel, including an array of device areas, each device area having a plurality of contacts exposed on a bottom surface of the substrate panel, a plurality of wire bonding landings exposed on a top surface of the substrate panel, and lead segments electrically coupling selected wire bonding landings to associated contacts; and

a dielectric material that fills spaces between adjacent lead segments.

2. The substrate panel of claim 1 wherein a top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings, and the bottom surface of the dielectric material is substantially coplanar with the bottom surface of the substrate panel and the lead contacts.

3. A substrate panel as recited in claim 1 wherein the wire bonding landings are thinner than the substrate panel, such that the wire bonding landings are not exposed on the bottom surface of the substrate panel.

4. A substrate panel as recited in claim 1 wherein at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.

5. A substrate panel as recited in claim 1 wherein the device areas are arranged in at least one two dimensional array.

6. A substrate panel as recited in claim 1 wherein the lead-frame further comprises a matrix of tie bars, the tie bars being positioned between adjacent device

areas in the two dimensional array of device areas and configured to support the lead segments.

7. A substrate panel as recited in claim 1 wherein each device area further includes a die attach pad, the die attach pad being exposed on the top surface of the substrate panel.

8. A substrate panel as recited in claim 7 wherein the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel.

9. A substrate panel as recited in claim 7 wherein at least one of the wire bonding landings is electrically coupled to the die attach pad.

10. A substrate panel as recited in claim 7 wherein at least one of the contacts is located between the wire bonding landings and the die attach pad.

11. A substrate panel for use in semiconductor packaging, comprising:

a lead-frame panel including a two dimensional array of device areas, each device area having a plurality of contacts exposed on a bottom surface of the substrate panel, a plurality of wire bonding landings exposed on a top surface of the substrate panel, and lead segments electrically coupling selected wire bonding landings to associated contacts; and

a dielectric material that fills spaces between adjacent lead segments, wherein a top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings, and a bottom surface of the dielectric material is substantially coplanar with the bottom surface of the substrate panel and the lead contacts; and

wherein at least some of the wire bonding landings are thinner than the substrate panel, such that the thinner wire bonding landings are not exposed on the bottom surface of the substrate panel, and at least selected portions of the lead

segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.

12. A substrate panel as recited in claim 11 wherein each device area further includes a die attach pad, the die attach pad being exposed on the top surface of the substrate panel.

13. A substrate panel as recited in claim 12 wherein the contacts surround the die attach pad, and wherein the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel, the contacts and the posts being arranged in a two dimensional array.

14. A substrate panel as recited in claim 12 wherein at least one of the wire bonding landings is electrically coupled to the die attach pad.

15. A packaged integrated circuit, comprising:

a substrate having a device area and a thickness, the device area further including a plurality of contacts exposed on a bottom surface, a plurality of wire bonding landings exposed on a top surface, lead segments electrically coupling the wire bonding landings to associated lead contacts, and a first dielectric layer that fills spaces between adjacent lead segments;

a die mounted on the substrate, the die having a plurality of bond pads configured for electrical connection to the wire bonding landings;

a plurality of connectors for electrically connecting the plurality of bond pads to associated wire bonding landings; and

a second dielectric layer that encapsulates the die and the plurality of connectors.

16. A packaged integrated circuit as recited in claim 15 wherein the first and second dielectric layers are formed from substantially the same materials.

17. A packaged integrated circuit as recited in claim 15 wherein an upper portion of the first dielectric layer is substantially coplanar with the top surface of the substrate and the plurality of wire bonding landings, and a lower portion of the first dielectric layer is substantially coplanar with the bottom surface of the substrate and the lead contacts.

18. A packaged integrated circuit as recited in claim 15 wherein the wire bonding landings are thinner than the thickness of the substrate, such that the wire bonding landings are not exposed on the bottom surface of the substrate.

19. A packaged integrated circuit as recited in claim 15 wherein at least selected portions of the lead segments are thinner than the thickness of the lead-frame, such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate.

20. A packaged integrated circuit as recited in claim 15 wherein the substrate further includes a die attach pad surrounded by the lead contacts, the die attach pad being exposed on the top surface of the substrate.

21. A packaged integrated circuit as recited in claim 20 wherein the die attach pad has a plurality of posts that are exposed on the bottom surface of the substrate.

22. A packaged integrated circuit as recited in claim 20 wherein at least one of the wire bonding landings is electrically coupled to the die attach pad.

23. A packaged integrated circuit as recited in claim 20 wherein at least one of the contacts is located between the wire bonding landings and the die attach pad.

24. A method of packaging an integrated circuit die, comprising:

receiving a substrate having a device area and a thickness, the substrate including a bottom surface, a plurality of wire bonding landings exposed on a top surface, lead segments electrically coupling the wire bonding areas to associated lead contacts, and a first dielectric material deposited within spaces between adjacent lead segments;

attaching a semiconductor die to the device area, wherein the semiconductor die has a plurality of bond pads;

electrically connecting the bond pads to associated wire bonding areas; and

encapsulating the semiconductor die with a second dielectric material.

25. The method of claim 24 wherein said receiving further comprises receiving a substrate having a first dielectric material, the first dielectric material including an upper portion that is substantially coplanar with the top surface of the substrate, and a lower portion that is substantially coplanar with the bottom surface of the substrate and the lead contacts.

26. The method of claim 24 wherein said receiving further comprises receiving a substrate including lead segments, wherein at least selected portions of the lead segments are thinner than the thickness of the substrate such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate.

27. The method of claim 24 wherein said encapsulating includes encapsulating the semiconductor die with a second dielectric material that is substantially the same as the first dielectric material.

28. The method of claim 24 wherein said receiving includes receiving a substrate having a device area with a die attach pad, the die attach pad being surrounded by the lead contacts and exposed on the top surface of the substrate.

29. The method of claim 28 wherein said receiving includes receiving a substrate having a device area with a die attach pad, the die attach pad having a plurality of posts exposed on the bottom surface of the substrate.

30. The method of claim 28 wherein said receiving includes receiving a substrate having a device area with a die attach pad, the die attach pad being electrically coupled to at least one of the wire bonding landings.